

# VLSI DESIGN FOR PULSE COMPRESSION SEQUENCES

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*Abstract: Pulse compression is defined as a technique that allows the radar to utilize a long pulse to achieve large radiated energy but simultaneously obtaining the range-resolution of a short pulse. Pulse compression signals can be divided into linear frequency modulation (LFM) signals, non-linear frequency modulation (NLFM) signals and phase-coded (PC) signals. This paper presents the VLSI design of the Pulse compression sequences using Phase Coding (PC) Technique based on Discrimination Factor using an efficient Modified Genetic Algorithm.*

*Keywords: Discrimination Factor, Modified Genetic Algorithm, Phase Coded Signals/Technique, Pulse Compression.*

## 1. INTRODUCTION

Pulse compression sequences with low auto correlation functions with one main peak and very small side peaks are important in telecommunications, radar and spread spectrum applications. This real time signal processing is designed using VLSI by writing code in VHDL and doing synthesis with Xilinx12.1. The targeted device selected here is Spartan-3 xc3s5000fg900-5.

## 2. FOUR PHASE CODE SEQUENCE SET

The problem of obtaining long sequences with peaky autocorrelation is an optimization problem. To overcome the signal design problem it is suggested to employ sequences like Binary and Poly phase sequences.

The Poly phase sequence of length N bits is represented by a complex number sequence as in eqn(1).

$$\{s(n) = e^{j\phi_m(n)}, \quad n = 1, 2, \dots, N\} \quad (1)$$

Where  $\phi_m(n)$  is the phase of nth bit in the sequence and lies between 0 and  $2\pi$ .

Considering a Poly phase sequence s with code length N, we can represent the phase values of s as in eqn(2).

$$S = [\phi_m(1), \phi_m(2), \phi_m(3), \dots, \phi_m(N)] \quad (2)$$

Therefore the Four phase code set S with code length N, set size L, and distinct phase number M can be represented as in eqn(3).

$$S(L,N,M) = \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_L \end{bmatrix} = \begin{bmatrix} \phi_1(1) & \phi_1(2) & \phi_1(3) & \dots & \phi_1(N) \\ \phi_2(1) & \phi_2(2) & \phi_2(3) & \dots & \phi_2(N) \\ \vdots & \vdots & \vdots & \dots & \vdots \\ \phi_L(1) & \phi_L(2) & \phi_L(3) & \dots & \phi_L(N) \end{bmatrix} \quad (3)$$

### 3. NEED FOR FPGA IMPLEMENTATION

The synthesis of Pulse Codes is a computationally-intensive procedure for which

1. Pure software solution is not practical as it is a “Non-Real-time” solution. Only identification of the Pulse compression sequences is possible and the identified pulse coded signal cannot be transmitted or received as there is no hardware.
2. FPGA implementation combines “Hardware performance” with the “Flexibility” of Software.
3. Reconfigurability of such devices allows code modifications after the hardware is Configured.

The proposed architecture is a single chip solution for both identification and Generation of the pulse compression sequences.

4. Vlsi design for pulse compression using phase coded sequence based on Modified Genetic Algorithm: As the sequences length increases it consumes more time and hence global optimization techniques like genetic algorithm, simulation annealing algorithm and so on are implemented in the software.

The main advantage of implementation using Hardware based Genetic Algorithm is its inherent speed over Software based methods. This speed is due to Flexibility of Reconfigurability and Reprogrammability of FPGA.

The VLSI architecture for the implementation of MGA with optimal pulse codes is shown in Fig 1.

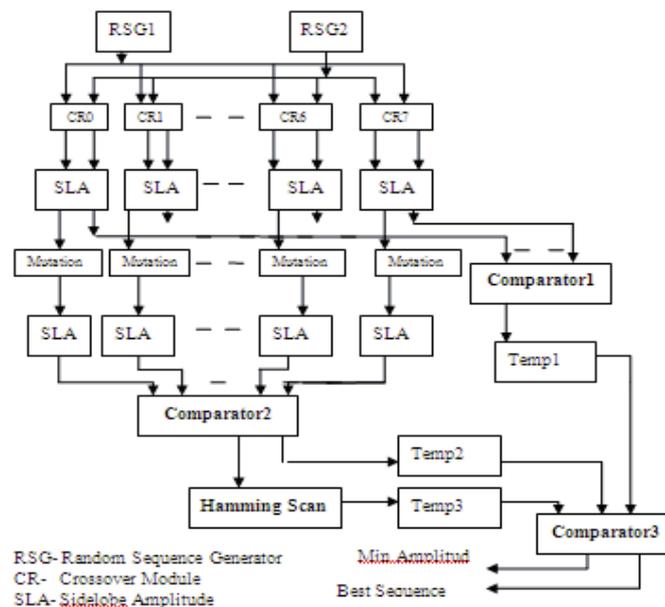


Fig 1. VLSI Architecture of Modified Genetic Algorithm with optimal pulse codes

The Proposed Modified Genetic Algorithm (MGA) combines the good methodologies of two algorithms like global minimum converging property of Genetic Algorithm (GA) and fast convergence rate of Hamming Scan Algorithm (HSA).

This VLSI architecture consists of mainly the Random Sequence Generator (RSG), Crossover Module (CR), Mutation Module, and Fitness Function Evaluation Module.

For all these sequences MGA calculates the Side Lobe Amplitude (SLA) values and identifies & holds the sequence with minimum side lobe amplitude.

This is as explained in four steps below.

In the first step the crossover module is used to perform the crossover operation on the two randomly generated sequences say as R1 and R2, by exchanging parts of their sequences two new sequences will be formed say R1',R2'. Swapping of R1, R2 can be performed by selection line of the Multiplexer. The Fitness function of R1' and R2' is calculated with side lobe amplitude calculator and compare these amplitudes with comparator. The best sequence and Minimum side lobe amplitude can be obtained from the comparator.

In the second step the best sequence from the crossover module is stored in Register R and First bit of the sequence is muted. The Fitness function of muted sequence is calculated with SLA and compares these amplitudes with comparator. The best sequence and Min. side lobe amplitude can be obtained from the comparator and stored in Temporary register.

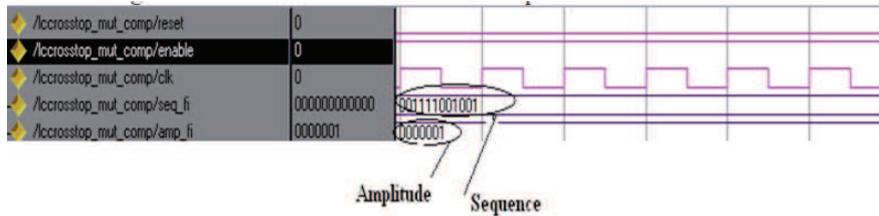
In the third step of hamming scan algorithm each Alphabet in the sequence is muted with all other 3 possible alphabets and corresponding side lobe amplitude values computed. The Comparator again compares the side lobe amplitude values and identifies the minimum amplitude and the corresponding sequence is reflected to the output Register.

In the final step side lobe amplitudes obtained after crossover, mutation and hamming scan operations are compared and are compared the sequence with the lowest side lobe amplitude will be the best sequence among all generated after each operation.

## 5. RESULTS & DISCUSSIONS:

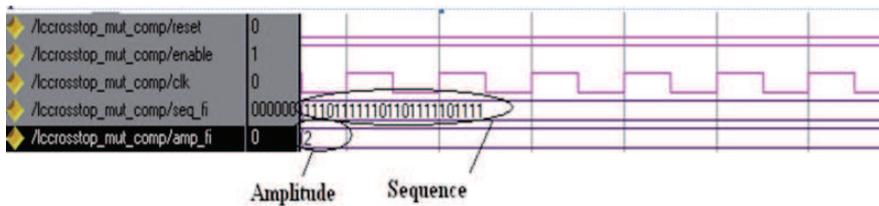
### A. Simulation Waveforms (Sequence Length (SL) 4 and 8):

The simulation waveforms for the Four phase Pulse compression sequence of length 4 are shown in Fig 2. It can be seen that Four phase sequence based on the lowest side lobe amplitude is 1, among all the side lobe amplitudes 001 111 001 001 (+1 -j +1 +1). Therefore the good Discrimination Factor of this sequence is 4.



**Fig 2 :** waveform for identification of best Four phase Pulse Compression Sequence of Length 4 using MGA.

The simulation waveforms for the Four phase Pulse compression sequence of length 8 are shown in Fig 3. It can be seen that Four phase sequence based on the lowest side lobe amplitude is 2, among all the side lobe. Therefore the good Discrimination Factor of this sequence is 4.



**Fig 3 :** waveform for identification of best Four phase Pulse Compression Sequence of Length 8 using MGA.

**B. Post-Synthesis Simulation (Sequence Length 4 & 8)**

After the synthesis, the synthesis tool generates a complete net-list of target hardware components and their timings. The details of gates used for the implementation of the design are described in this netlist. The netlist also includes wiring delays and load effects on gates used in the post-synthesis design.

The netlist output is made available in various netlist formats including VHDL. Such a description can be simulated and its simulation is referred as Post Synthesis simulation. Timing issues, Determination of proper clock Frequency and race and hazard considerations can only be checked by a post synthesis simulation run after a design is synthesized.



**Fig4:** Post-Route Simulation waveform for Four phase Pulse Compression Sequence of Length 4



**Fig5: Post-Route Simulation waveform for Four phase Pulse Compression Sequence of Length 8.**

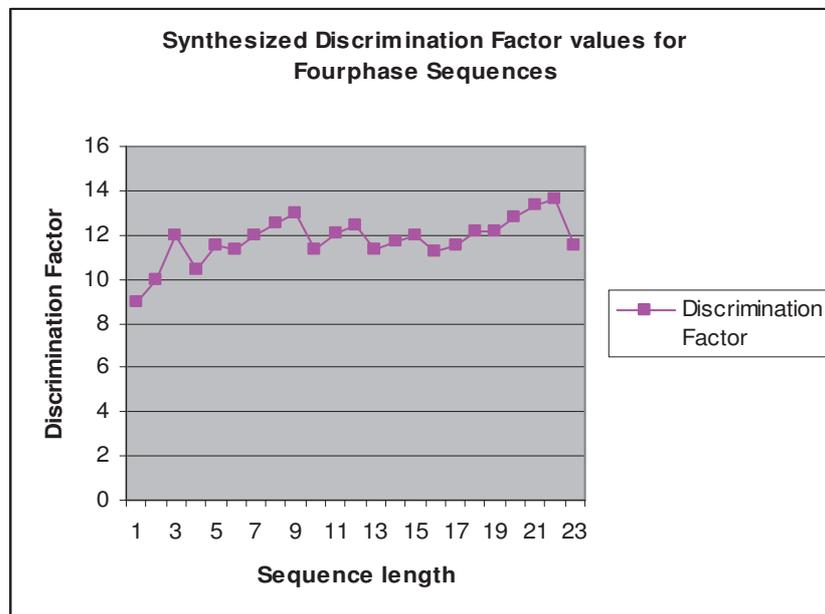
**C. Calculation of Discrimination Factor for Four Phase Pulse Compression Codes:**

The discrimination Factor for Four phase pulse compression sequences for different lengths have been represented in the Table 1

**Table 1: Synthesized Discrimination Factor values for Four phase Sequences**

Len	8	9	10	12	14	15	16	17
DF	5.66	6.36	7.07	8.48	9.89	15	11.3	8.50

The Graphical representations of Four phase for different lengths is as shown in Fig6.



**Fig 6: Graphical representations of Four phase for different lengths**

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## 6. REFERENCES

1. Pei-Yin Chen, Ren-Der Chen, Yu-Pin Chang, "Hardware Implementation For a Genetic Algorithm", *IEEE Trans. Instrumentation and Measurement*, vol. 57, NO.4, April 2008
2. N. Balaji, Dr. K. Subba Rao, M. Srinivasa Rao, "FPGA Implementation of Four phase Pulse Compression Sequences using FPGA" Proc of Third Innovative Conference on Embedded Systems, Mobile. Communication and Computing (ICEMC2) 11<sup>th</sup> - 14<sup>th</sup> August, 2008.
3. T. Helleseth and P. V. Kumar, "Sequences with low correlation," in *Handbook of Coding Theory*, V. S. Pless and W. C. Huffman, Eds. Amsterdam, The Netherlands: Elsevier, 1998.
4. Lewis, B.L. and Kretschmer, F.F. (1980) A new class of pulse compression codes and techniques. Washington, DC, Naval Research Laboratory, NRL Report 8387, Mar. 26, 1980.
5. Peter Browein, Ron Ferguson: 'Polyphase sequence with low autocorrelation. *IEEE Trans. Inf. Theory* 2005 IT-51(4)1564–1567.
6. W.H.Mow and S.Y.R.Li, "Aperiodic autocorrelation and cross correlation of polyphase sequences," *IEEE Trans. Inform. Theory*, vol. 43, pp. 1000–1007, May 1997
7. Pei-Yin Chen, Ren-Der Chen, Yu-Pin Chang, "Hardware Implementation For a Genetic Algorithm", *IEEE Trans. Instrumentation and Measurement*, vol. 57, NO.4, April 2008
8. M. K. Simon, J. K. Omura, R. A. Scholtz, and B. K. Levitt, *Spread Spectrum Communications*. Rockville, MD: Computer Sci. 1985, vol. 1.

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