A NEW ARCHITECTURE FOR LOW POWER ROW BYPASSING MULTIPLIER USING RCA

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Abstract : In this paper a new technique for the architecture of the bypassing multiplier for low power and high speed is introduced. The basic idea is to bypass blocks of logic when their function is not required, using low delay and area overhead components using TG gates. While this technique offers great dynamic power savings mainly in array multipliers, due to their regular interconnection scheme, it misses the reduced area and fast speed advantages of tree multipliers. 8x8 Row bypassing multiplier is divided into two 8x4 and 4x8, when these are combined at middle of the final adder compressor is used to enhance the speed of the row bypassing multiplier. HSPICE is used to evaluate the performance of the multiplier for 130 nm at 1.8 Volts.

Introduction : As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amounts of energy. While performance and power remain to be two major design goals, power consumption has become a critical concern in today's VLSI system design. The need for low-power VLSI systems arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited.

Multiplication is a fundamental operation in most arithmetic computing systems. To achieve high execution speed, parallel array multipliers are widely used. These multipliers tend to consume most of the power in DSP computations, and thus power-efficient multipliers are very important for the design of low-power DSP systems. Bypassing technique is a well known technique to reduce power in parallel array multipliers 1]. The primary power reductions are obtained by tuning off MOS components through multiplexers when the operands of multiplier are zero. Analysis of the conventional DSP applications shows that the average of zero input of operand in multiplier is 73.8 percent. Therefore, significant power consumption can be reduced by the proposed bypassing multiplier 2, 3].

1. Power Consumption In Cmos Circuits

Power is the most important parameter in digital circuits to fabricate chips and portable devices. CMOS technology is used in digital circuits due to its less power consumption. Power consumption in CMOS circuits can be divided into dynamic and static power consumption shown in equation (1).

$$Ps = \alpha f_{clk} C_L V_{DD}^2 + I_{SC} V_{DD} + I_{leakage} V_{DD} \quad (1)$$

Where α is the switching activity, f_{clk} is the clock frequency, C_L is the output capacitance, V_{DD} is the supply voltage, I_{SC} is the short circuit current, and $I_{leakage}$ is the leakage current. In micrometer technology dynamic power is the dominant parameter while in the submicron technology, leakage current is the most dominant parameter in total power. The concentration of this paper is on dynamic power reduction 6].

2. Parallel Multiplier

A serial multiplier consumes less power but due to ripple, delay will be more. In parallel multiplier delay is less but high complex circuitry it consumes more power.

Consider the multiplication of two unsigned n-bit numbers, where X = x_{n-1}, x_{n-2}, ... x_o is the multiplicand and Y = y_{n-1},y_{n-2}, ...,y_o is the multiplier. The product of these two bits can be written as 7].

$$P = \sum_{i=0}^{n-1} X_i \sum_{j=0}^{n-1} Y_j 2^{(i+j)} \quad (2)$$

Where

$$X = \sum_{i=0}^{n-1} X_i 2^i \quad \text{---Multiplicand}$$

$$Y = \sum_{j=0}^{n-1} Y_j 2^j \quad \text{------ Multiplier}$$

a_3	a_2	a_1	a_o	Multiplicand
b_3	b_2	b_1	b_o	Multiplier

PP

b_3a_o	b_2a_o	b_1a_o	b_oa_o				
		b_3a_1	b_2a_1	b_1a	b_oa_1		
	b_3a_2	b_2a_2	b_1a_2	b_oa_2			
b_3a_3	b_2a_3	b_1a_3	b_oa_3				
P7	P6	P5	P4	P3	P2	P1	Po

Fig 1. Multiplication Architecture

3. Bypassing Technique

4.1 Row Bypassing Technique

A low-power multiplier design may disable the operations in some rows to save power. If bit b_j is 0, all partial products a_ib_j, $0 \le i \le n-1$, are zero. Therefore, the additions in the corresponding row can be bypassed. The row bypassing multiplier (RBM) 4, 5] is shown in Fig. 2. Each cell in the carry save adder (CSA) array is designed with three tri-state gates and two multiplexers. Let $b_2 = 0$. In this case, the CSA in the second row can be bypassed, and the outputs from the first row are fed directly to the third row CSA. However, since the rightmost FA in the second row is disabled, it does not execute the addition and thus the output is not correct. To remedy this problem, an extra circuit must be added.

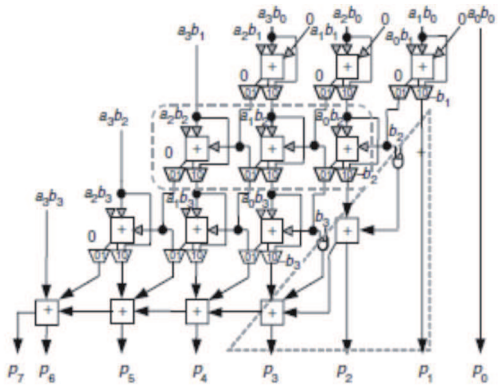

Fig. 2 Row Bypassing Multiplier using CSA

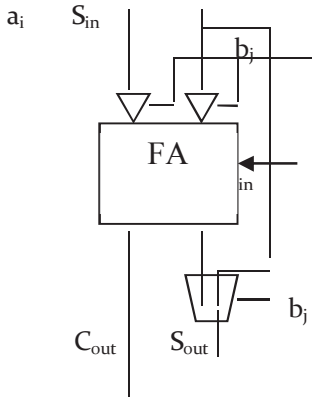

Fig. 3 Column Bypassing Cell

4. Row bypassing multiplier with CSA

A ripple carry adder (RCA) adder is adopted with bypassing ability in each row of adders. The reason of adopting RCA adder instead of CSA adder is to achieve parallel architecture. The two tri-state buffers are placed at two inputs of full adder to disable the operation of full adder when b_j is 0. The tri-state buffer is designed by transmission gate (TG). The multiplexer is placed at the sum output of full adder.

The value of sum can be selected from the bypassing value or sum output of full adder according to the value of b_j. The proposed design does not need to add multiplexer for carry output and tri-state buffer for carry input of full adder. The reason is that two inputs of full adder in jth row need to be disabled while the value of b_j is 0. Thus carry outputs of the full adders in the same row cannot be changed since two out of three-input full adder is disabled. Thereby, full adder only needs two tri-state buffers and one multiplexer as shown in Fig. 3. Moreover an AND gate is inserted into the last carry output in each row of full adder for correcting output when the value of b_j is 0. Therefore, significant portion of extra hardware can be saved without degrading speed performance. In addition, power consumption also can be reduced as a result of reduced hardware activities. Fig.4 shows 4x4 row based bypassing multiplier with RCA.

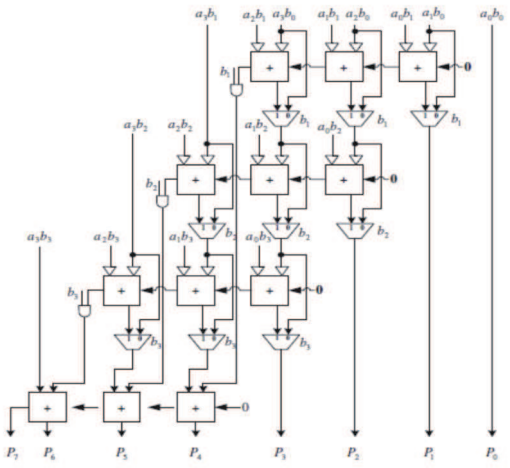

Fig.4 A 4x4 row bypassing multiplier based on RCA.

For an example of 8x8 multiplication, two 8x4 bypassing multiplier based on RCA. The partial sums and carry output from these two 8x4 multipliers can be computed simultaneously. Note that the final stage adders consist of RCA adders in both sides and CSA adders in the middle. In this configuration, the parallelism of the multiplier can be established. Furthermore, delay time of RCA multiplier can be shortened through this method. To enhance the performance of the row bypassing multiplier further more, with little expense of power a method is proposed. According this proposed method, a compressor is placed at where the CSA are placed in the design of 2]. The compressors are can boost the performance of the row bypassing multiplier at the middle of the design.

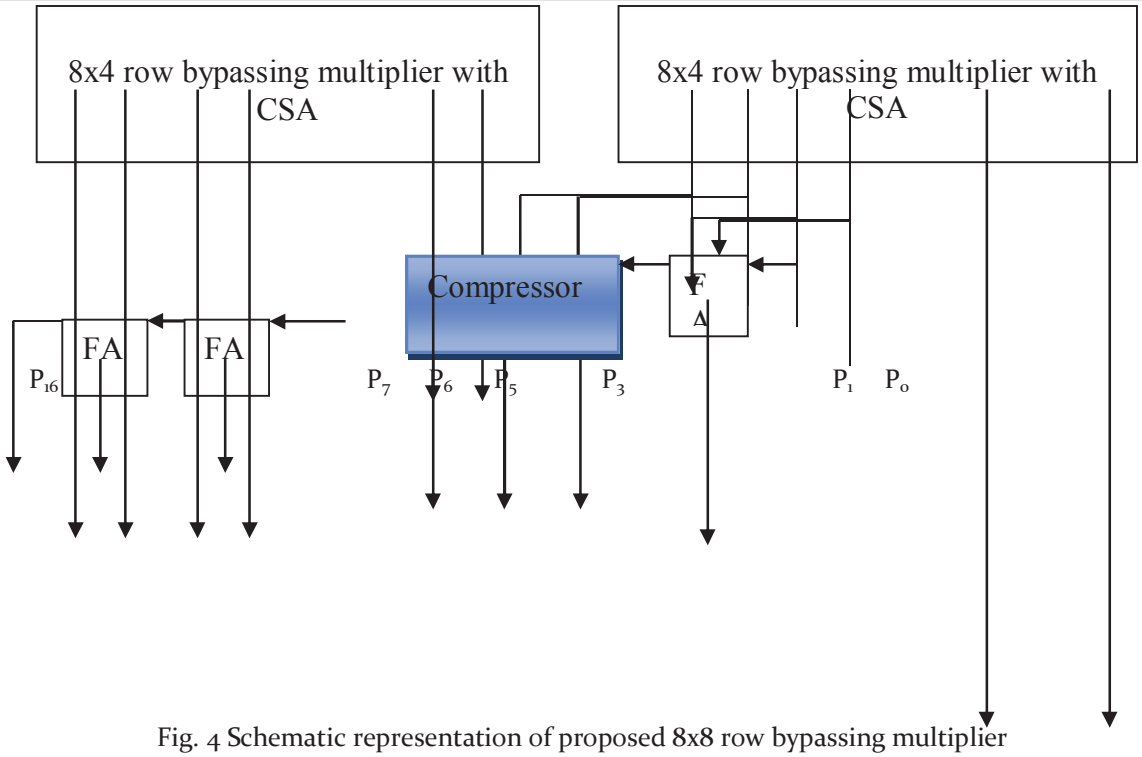

Fig. 4 Schematic representation of proposed 8x8 row bypassing multiplier

5. Simulation results

All the multiplier designs are implemented in Tanner EDA S-Edit. The generated netlist is simulated using Synopsys HSPICE with 130 nm technology for 1.8 Volts. 16-T full adder is used to implement the bypassing multipliers. TGCMOS, transmission function adder (TFA), 16-T and 14-T full adders 8]. 16-T is the energy efficient full adder.

Table 1. Total power consumption, propagation delay and EDP of the multipliers

Multiplier	Total power consumption	Propagation delay	Energy product delay (EDP)
4x4 RBM	7.52-03	9.73-09	7.11-19
4x4CRBM	7.60-03	3.48-08	9.20-18
8x8 CRBM with CSA	2.31-02	1.61-07	5.98-16
8x8 proposed	2.86-02	1.61-07	7.41-16

4x4 RBM consumes a total power of 7.52 mW and CSA RBM consumes 7.6 mW of power shown in Table 1. The proposed 8x8 row bypassing multiplier with compressor consumes little more power with improvement of speed at middle of the multiplier i.e at P_9, P_{10}, P_{11}, P_{12} etc. But the worst case delay is same as that of the multiplier CRBM with CSA 2].

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